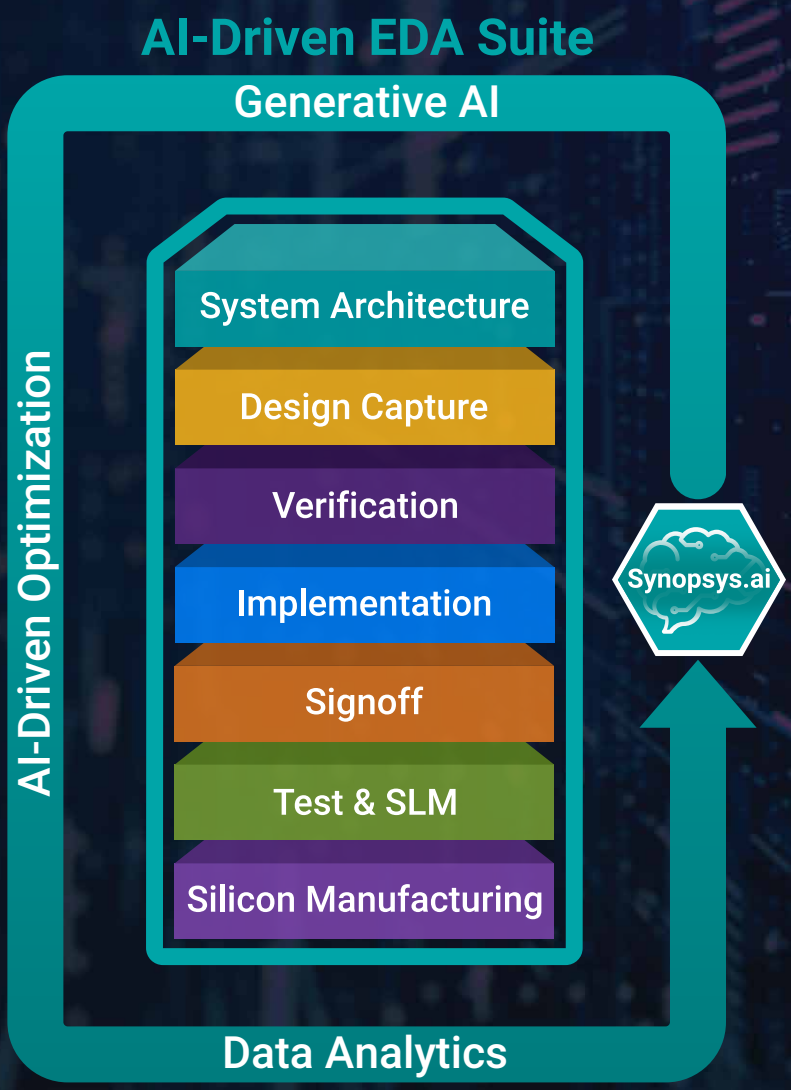
SYNOPSYS®

Synopsys.ai – Full Stack, AI-Driven EDA Suite

From System Architecture to Design and Manufacturing



Overview

The rapid and exponential increase in chip design complexity is creating significant hurdles for the semiconductor industry. Companies must contend with the challenges posed by the march to angstroms, multi-die integration, and node migration, along with aggressive time-to-market targets, increasing manufacturing test costs, and the global engineering resource crunch. Advancements in artificial intelligence (AI) for electronic design automation (EDA) can address these challenges head on.

Synopsys.ai™, the industry's first full stack, AI-driven EDA suite's, is delivering significant quality or results (QoR) and productivity improvements across the entire stack. The suite's sustained differentiation to the chip design process includes comprehensive AI-driven design optimization, data analytics and generative AI capabilities. As the pioneer in AI-driven design, Synopsys.ai accelerates the chip design workflow by enabling companies to build more chips faster in the face of systemic complexity, shrinking talent shortages, and increased industry demands.

Comprehensive Generative AI Solutions

Synopsys will enable chip designers to achieve unprecedented productivity gains with the introduction of generative AI capabilities across the EDA stack, including:

- Collaborative capabilities with Synopsys.ai Copilot that provide engineers with guidance on tool knowledge, analysis of results and enhanced EDA workflows
- Generative capabilities to expedite development of RTL, formal verification assertion creation, and UVM testbenches
- Fully autonomous capabilities to enable end-to-end workflow creation from natural language spanning architecture to design and manufacturing

Powered by large language models (LLMs), Synopsys.ai generative AI capabilities can be deployed in any on-prem or cloud environment.

AI-Driven Design Optimization

Design engineers looking to reach the best power, performance, and area (PPA) targets can utilize the Synopsys Design Space Optimization (DSO.ai™) solution. Verification engineers can achieve higher quality verification coverage faster with the Synopsys Verification Space Optimization (VSO.ai™) solution. Test engineers faced with the challenge of reducing the number of test patterns while optimizing defect coverage can employ the Synopsys Test Space Optimization (TSO.ai™) solution. Analog design engineers can use Synopsys Analog Space Optimization (ASO.ai™) to improve analog design performance and robustness by optimizing complex analog designs across multiple testbenches and hundreds of PVT (process, voltage, temperature) corners to quickly converge on the optimal design points that meet engineering specifications. Additional technologies included with Synopsys ASO.ai enable designers to rapidly migrate analog designs across technology nodes.

Design Space Optimization—Synopsys DSO.ai

Complexity brought on by advanced process nodes have opened the door to challenges in achieving optimal power, performance, and area. Manual methods are no longer viable given shrinking market windows. The need to drive for better

Figure 1: DSO.ai provides unbeatable PPA results and the fastest time to design

Synopsys DSO.ai, the industry's first autonomous artificial intelligence application for chip design, searches for optimization targets in very large solution spaces of chip design, utilizing reinforcement learning to enhance power, performance, results faster is increasing and traditional methods cannot keep pace often resulting in months of tuning using 100s of trials. Even then, results are not optimal. Synopsys DSO.ai can help.

Synopsys DSO.ai, the industry's first autonomous artificial intelligence application for chip design, searches for optimization targets in very large solution spaces of chip design, utilizing reinforcement learning to enhance power, performance, and area. RTL-to-GDSII full flow optimization unlocks PPA potential across both logical and physical domains. Breakthrough reinforcement learning engines can explore trillions of design recipes. These models continue to train and accelerate convergence throughout the design cycle and bleed over to impact efficiency and productivity on iterative designs.

Synopsys DSO.ai is an industry award-winning solution deployed by 9 out of 10 semiconductor companies. Users have reported productivity enhancements of more than 3x, power reductions of up to 15%, and substantial die size reductions. DSO.ai helps companies surpass the most challenging goals in chip design and reach new levels of productivity.

Verification Space Optimization—Synopsys VSO.ai

Logic and functional issues that undermine the readiness of SoCs require extensive verification that can quickly evolve into an endless verification and debug loop. Chip verification engineers need to check each of the design state spaces to ensure that the final SoC design will work. The number of design state spaces in which a digital design can operate is nearly infinite, making it virtually impossible for humans to check each of these spaces to validate that the design will function as intended. Achieving full verification coverage is a daunting if not impossible task using traditional methods.

The traditional coverage closure flow requires verification engineers to manually define coverage and stimulus, often running 1000's of regressions with unknown ROI. After collecting the coverage data, manual analysis of the enormous data set only leads to minimal insights. To close coverage, tests must be manually biased or directed tests must be written which is labor intensive and slow and can still lead to bug escapes.

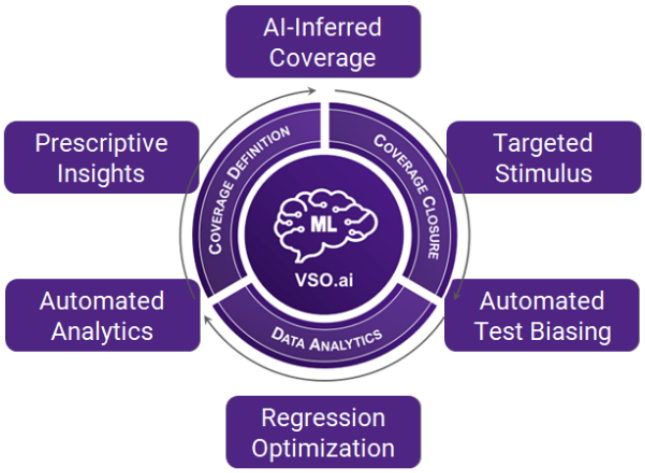


Figure 2: VSO.ai delivers faster, higher coverage closure and analytics

Synopsys VSO.ai revitalizes the coverage process by using AI to examine the RTL and infer coverage while also highlighting areas where coverage is needed, ultimately helping verification engineers reach coverage targets faster and find more bugs. Regressions are optimized so high ROI tests are run first and analysis is automated to define prescribed insights. Customers report achieving up to 10x improvement in reducing functional coverage holes and up to 30% increase in IP verification productivity using AI-driven verification with Synopsys VCS® functional verification solution.

Test Space Optimization—Synopsys TSO.ai

Growing design complexity and size also weigh down the silicon test process. Defect coverage, pattern count (which correlates directly to testing cost), and runtime are three key metrics to consider when evaluating the results from an automatic test pattern generation (ATPG) tool.

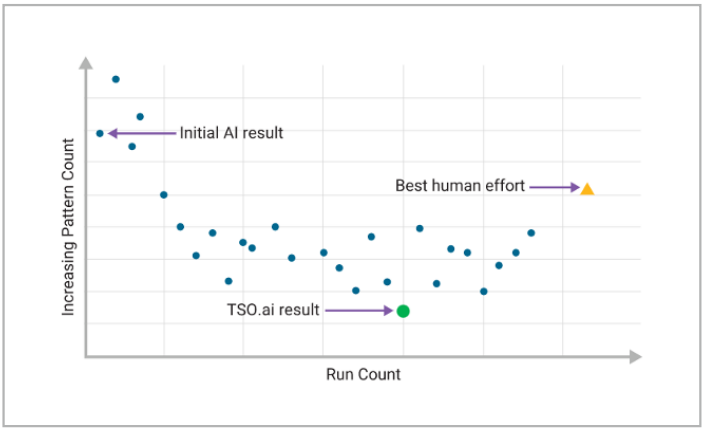


Figure 3: Optimal pattern count achieved using TSO.ai

Traditionally, optimizing for one of these metrics (typically by hand) negatively impacts the others. Someone who is new to ATPG may not have a strong sense of how to tweak the tool to generate the desired program results. Conversely, someone with a lot of experience may have biases that cause tool set up to achieve a certain result, which may not prove optimal for a new design.

Synopsys TSO.ai is the industry's first autonomous AI application for semiconductor test to minimize test costs and time-to-market for today's complex designs. TSO.ai automatically searches for an optimal solution in a large test search space to minimize pattern count and ATPG turn-around time reducing test costs dramatically and accelerating time to results.

Analog Space Optimization—Synopsys ASO.ai

There is a significant productivity gap when we compare traditional analog workflows which are highly manual and iterative with digital workflows that are typically automated. Synopsys ASO.ai brings a rich set of AI-powered analog automation features and solutions to improve productivity in analog design, simulation, verification, and implementation workflows. These new AI-based automations help analog design teams re-use decades of knowledge and experience for the development of state-of-the-art Analog IPs.

Synopsys ASO.ai introduces these new AI-based workflows:

Analog Design Migration—Rapid migration of hierarchical analog IPs across technology nodes including automatic schematic migration and knowledge-based automatic layout migration.

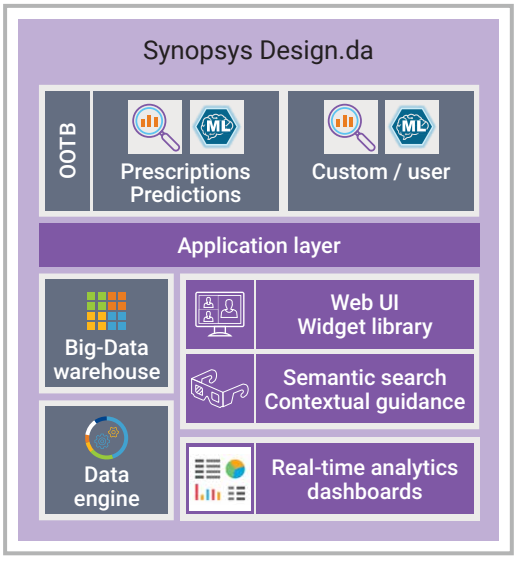
Layout-aware design optimization—Multi-objective optimization agent that learns while it runs, helping engineers center and further optimize analog design simultaneously across hundreds of PVT corners and across multiple tests. The AI-based optimizer can work on pre-layout and post-layout parasitic netlists to quickly converge and meet design specifications.

Intelligent simulation analysis—Aid engineers to quickly understand intricate signal-level behavior in a massive corner and multi-testbench simulations dataset that cannot otherwise be caught in an expression-based simulation analysis and hard to identify by viewing waveforms.

Synopsys ASO.ai automation workflows aim to improve designers' Turnaround Time (TaT) and reduce Cost-of-Results (CoR) while improving Analog design Quality-of-Results (QoR).

Full-Scale AI-Driven Data Analytics

Engineering teams can now harness the vast amounts of data collected from design, manufacturing, test, and in-field operations with a comprehensive AI-driven data analytics continuum for every stage of IC chip development. The Synopsys EDA Data Analytics solution unlocks, connects, and analyzes vast amounts of data to increase productivity across the full design-to-silicon lifecycle. Synopsys Design.da uncovers actionable design insights that accelerate the design process. Synopsys Fab.da improves fab yield and throughput enabling faster ramp and more efficient high-volume manufacturing (HVM). Synopsys Silicon.da automatically highlights silicon data outliers for improved chip quality, yield and throughput. A consolidated view of data automates root cause analysis enabling engineers to pinpoint areas of focus in real-time.



Design Analytics—Synopsys Design.da

The digital chip design flow carries with it an enormous wealth of untapped information regarding the health and status of your SoC design. The ability to efficiently mine this data provides chip designers with comprehensive visibility and actionable insights to uncover PPA opportunities.

Synopsys Design.da is the industry's first comprehensive data-visibility and machine intelligence-guided design optimization and signoff closure solution. The solution leverages vast datasets to bring unmatched productivity and a better, faster, and smarter way to design. Synopsys Design.da presents a holistic view of all project data and then efficiently and autonomously siphons metrics data while also intelligently curating the associated analysis data. It transforms and loads the data into always-on, industry-standard databases. Synopsys Design.da performs analysis not only to show what is happening but also why it is happening. The solution automatically classifies design trends, identifies limitations, and provides prescriptive guided root-cause analysis across the entire design flow.

Process Control Analytics—Synopsys Fab.da

Like the digital chip design flow, the manufacturing process creates volumes of data. The data collected during design, mask synthesis, process and device modeling, defect management, product testing, and cloud implementation goes largely unused. However, this data hides insights that can have significant productivity and quality implications.

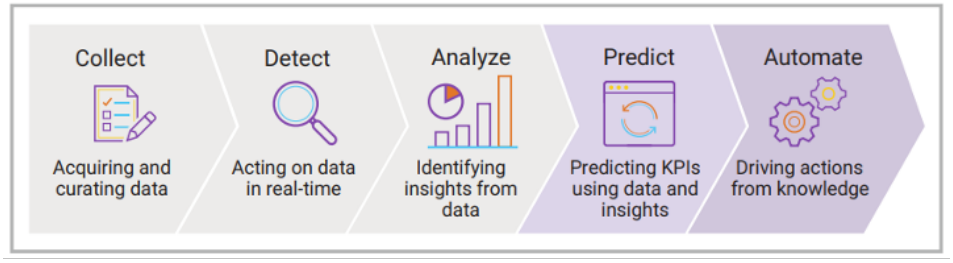


Figure 4: Synopsys Fab.da Flow

Synopsys Fab.da is an AI-driven comprehensive process analytics and control solution. The solution enables customers to fully harness the immense potential harbored within the volumes of fab equipment process control data. Fab engineers are able to generate actionable insights and improve operational excellence within semiconductor fabs.

Synopsys Fab.da provides an adaptable and robust platform capable of scaling to collect, manage, analyze and adapt data. It is designed to seamlessly accept petabytes of data from diverse sources, encompassing product design, equipment sensors, fab operations, and product testing. This data continuum ensures a comprehensive and accurate foundation for analytics

to simultaneously monitor equipment health, optimize process flows, rapidly identify underlying causes of failure, and predict outcomes to effectively mitigate manufacturing risks. As an advanced manufacturing platform, Synopsys Fab.da unifies disparate data elements into a singular, cohesive platform that continuously operates 24/7 avoiding the time-consuming and sub-optimal utilization of multiple analytics solutions. It adeptly meets the stringent data analytics demands of modern semiconductor fabs while managing the complete data lifecycle to drive insightful and data-powered decisions. Synopsys Fab.da helps to achieve faster process ramp and maximize product quality and fab yield.

Production Analytics—Synopsys Silicon.da

Semiconductor design, manufacturing and system deployment are being challenged on many fronts due to process variability, device aging effects, ever increasing performance expectations, and the continued reduction in time to volume. Synopsys is leading the industry to solve these challenges with its Synopsys Silicon.da solution.

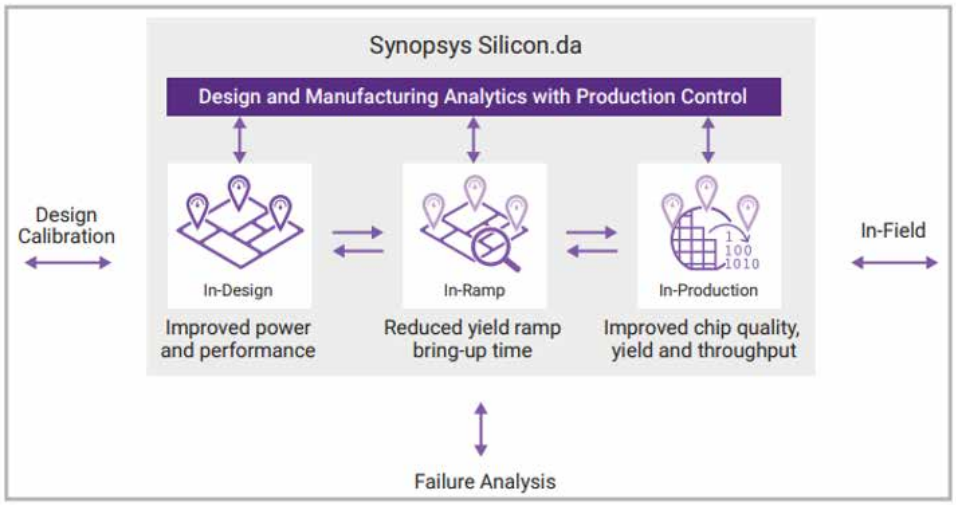


Figure 5: Actionable Insights Throughout the Silicon Life Cycle with Synopsys Silicon.da Analytics

Synopsys Silicon.da is a unique analytics solution spanning design and product manufacturing phases. The solution provides actionable insights through the use of powerful analytics and automatically highlights silicon data outliers to enable engineering teams to quickly identify and correct underlying issues in the semiconductor supply chain. Environmental, structural and functional monitors enable deep insights from SoC manufacturing to in-field systems. Meaningful data is gathered at every opportunity for continuous analysis and actionable feedback. Synopsys Silicon.da boosts productivity by consolidating analytics into a single environment while being able to process and analyze order of magnitude more silicon data compared to other approaches. It also enables engineering teams the ability to leverage silicon design, production and sensor data to quickly determine how to improve key chip production metrics such as yield, quality, and throughput, while also improving key silicon operational metrics such as chip power and performance.

Summary

The Synopsys.ai EDA suite uses the power of AI to optimize silicon performance, accelerate chip design, and improve efficiency throughout the entire EDA flow to deliver leading PPA and yield. The hyperconverged AI-driven EDA stack quickly handles design complexity and takes over repetitive tasks such as design space exploration, verification coverage and regression analytics, and test program generation. Synopsys.ai's comprehensive data analytics solutions further boost productivity by harnessing untapped, actionable insights from the enormous amount of data collected throughout the development flow. With Synopsys.ai, engineering teams can focus on design innovation and spend less time getting to market.

For more information about Synopsys products, support services or training, contact your local sales representative or visit us on the web at: www.synopsys.com.